A New Voltage Control Method for Single-Phase PWM Inverters

Pekik Argo Dahono[1] & Een Taryana[2]

[1]School of Electrical Engineering and Informatics,
Institute of Technology Bandung, Bandung, Indonesia
[2]Department of Electrical Engineering,
University of Jenderal Achmad Yani, Bandung, Indonesia

Abstract. A new voltage control method for single-phase full-bridge PWM inverters that having an output LC filter is proposed in this paper. The proposed voltage controller has a capability to realize a zero steady-state output voltage error with fast response. The zero steady-state output voltage error is achieved by using a controller that is derived by using the virtual LC resonant circuit. Fast response is obtained by using a virtual resistance that is connected in parallel with the filter capacitor. The validity of the proposed method is verified by experimental results.

Keywords: *PWM inverter; virtual LC; virtual resistor.*

1 Introduction

A single-phase full-bridge PWM inverter is commonly used in low and medium power uninterruptible power supplies (UPS). In such applications, a fast and accurate output voltage control under various conditions is desirable. Various control techniques were developed for this purpose [1-6]. Most of these techniques, however, are difficult to implement and sensitive to parameter variations. At present, a zero steady-state output voltage error is usually obtained by using a complicated transformation of the phase variables into the ones in synchronous rotating reference frame. Such reference frame, however, is not available in the case of single-phase PWM inverters.

A new voltage control method for single-phase full-bridge PWM inverters is proposed in this paper. The proposed voltage controller has capability to realize a zero steady-state output voltage error with fast response without complicated transformation. To control the output voltage, a voltage control based on new virtual LC resonant circuit is proposed. By using the proposed control technique, a zero steady-state error can be achieved. In order to improve the output voltage response, a virtual resistor is connected in parallel with the output filter capacitor. Two types of virtual resistance are discussed in this

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paper. Experimental results show that the output voltage of single-phase PWM inverter can be controlled faster and accurately even under nonlinear loads.

2 Virtual LC Resonant Circuit

Figure 1 shows the scheme of single-phase full-bridge PWM inverter that is used in this investigation. An output LC filter is used to minimize the output harmonics. A standard double-loops controller is used to control the inverter. An inner current loop controller is used to control the filter inductor current. The inner current controller must be much faster than the outer voltage controller. A fast current controller using double-band hysteresis such as the one that was proposed by the author in [7] is used in this investigation. It is assumed here that the current controller is working properly: So that the actual filter inductor current can be assumed to be the same as the current reference. The outer voltage loop controller generates the current reference for the filter inductor current.

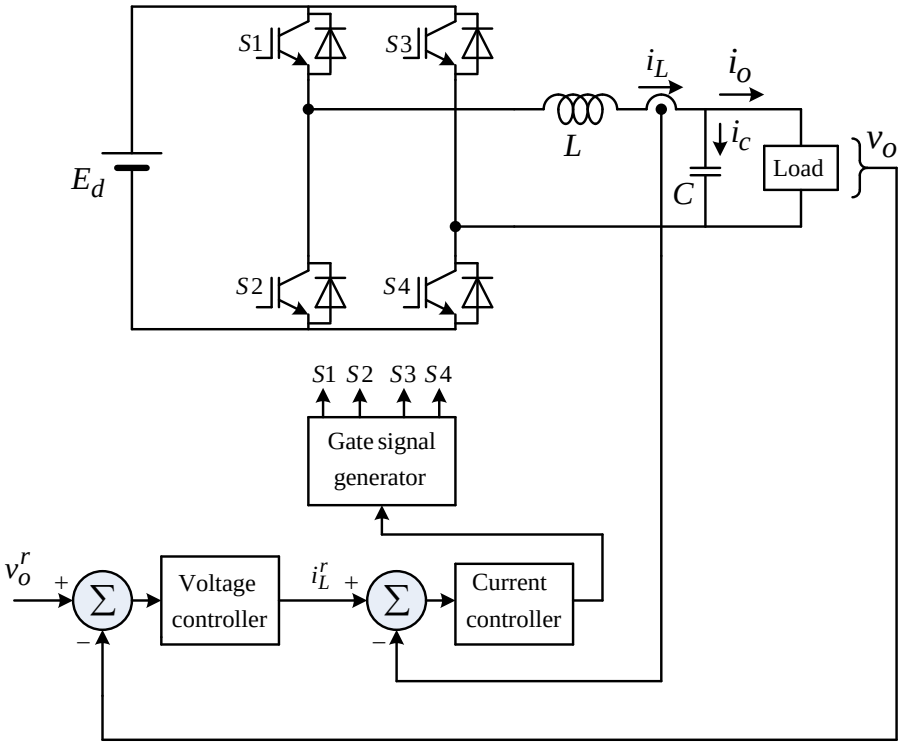


Figure 1 The scheme of PWM inverter with the associated controller.

Figure 2(a) shows the output side equivalent circuit of the inverter when the filter inductor current is assumed equal to the reference current. Figure 2(b) shows the block diagram of the system. Based on the block diagram in Figure 2(b), the output voltage response can be written as

$$V_o(s) = \frac{1}{sC} I_L^r(s) - \frac{1}{sC} I_o(s) \tag{1}$$

where *s* is the Laplace operator.

Based on the filter capacitor circuit in Figure 2(a), the capacitor current can be obtained as below:

$$I_c = I_L^r - I_o \tag{2}$$

The capacitor current can be separated into two components, that is,

$$I_c = \bar{I}_c + \tilde{I}_c \tag{3}$$

where $\bar{I}_c$ is the capacitor current component that generates the desired output voltage and $\tilde{I}_c$ is the capacitor current component that generates the output voltage error.

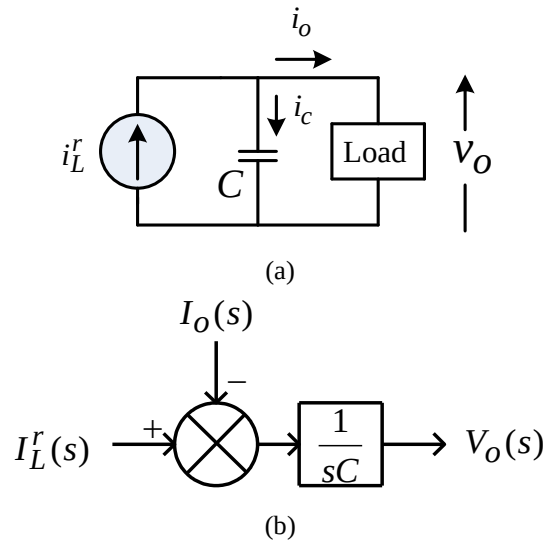


Figure 2 Load side equivalent circuit and its block diagram.

Figure 3(a) shows the equivalent circuit that showing how the output voltage error is generated by the current $\tilde{I}_c$. In order to eliminate the steady-state output voltage error, the current $\tilde{I}_c$ should not be allowed to flow through the filter capacitor. The current $\tilde{I}_c$ will be not flowing through the capacitor if a very low impedance path is available in parallel with the filter capacitor. A very low impedance path can be created by using a tuned series LC resonant circuit as shown in Figure 3(b). Figure 3(c) shows the block diagram that represents the system in Figure 3(b). If the LC resonant circuit is tuned at the desired fundamental output voltage frequency (e.g., 50 Hz) then no 50 Hz component of $\tilde{I}_c$ will flow through the filter capacitor. Under this condition, no output voltage error at 50 Hz is generated. Thus, we need a tuned series LC resonant circuit that gives response only to the undesired capacitor current or undesired output voltage components. The tuned series LC resonant circuit should not give response to the desired capacitor current or desired output voltage. Such tuned series LC resonant circuit cannot be realized by using real LC components. The required series LC resonant circuit can be implemented virtually by using software or analog electronic components. As shown in Figure 3(c), the input of the virtual LC resonant circuit is the undesired output voltage component. This voltage can be obtained as the actual output voltage minus the reference voltage as shown in Figure 3(d).

Based on Figure 3(d), the output voltage response can be obtained as

$$V_o(s) = \frac{\dfrac{1}{L_r C}}{s^2 + \omega_o^2 + \dfrac{1}{L_r C}} V_o^r(s) - \frac{s^2 + \omega_o^2}{sC\left(s^2 + \omega_o^2 + \dfrac{1}{L_r C}\right)} I_o(s) \qquad (4)$$

and the error response is

$$V_o^r(s) - V_o(s) = \frac{s^2 + \omega_o^2}{s^2 + \omega_o^2 + \dfrac{1}{L_r C}} V_o^r(s) + \frac{s^2 + \omega_o^2}{sC\left(s^2 + \omega_o^2 + \dfrac{1}{L_r C}\right)} I_o(s) \qquad (5)$$

where $\omega_o = 1/\sqrt{L_r C_r}$ is the resonant frequency of the LC circuit. If the LC resonant circuit is tuned at 50 Hz (ω_o=100π rad/s) then the output voltage and the error signal at this frequency can be obtained from Eqs. (4)-(5) as below:

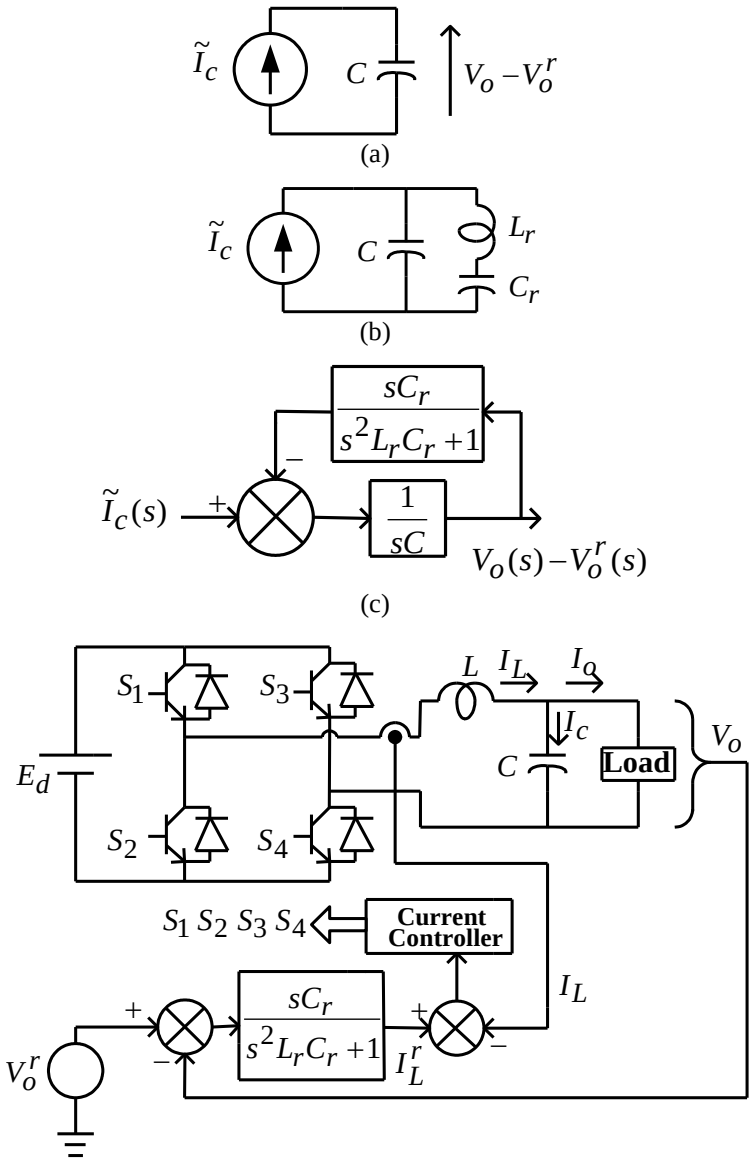


Figure 3 Development of voltage controller based on virtual LC resonant circuit.

$$V_o\left(j\omega_o\right)=V_o^r\left(j\omega_o\right) \tag{6}$$

$$V_o^r(j\omega_o)-V_o(j\omega_o)=0 \tag{7}$$

Thus, the 50 Hz component of the output voltage is equal to the 50 Hz component of the reference voltage. The error component of the output voltage at 50 Hz is equal to zero.

A similar controller was developed to control the input current of PWM rectifiers [8-11]. The difference is the existence of a differentiator in the numerator of controller in Figure 3(d).

3 Virtual Resistor

Though a voltage controller that is derived by using a virtual series LC resonant circuit can realize a zero steady-state output voltage error at the desired frequency, the controller has oscillatory response as indicated by Eq. (4). A simple way to damp the oscillation is by using a resistance that is connected in parallel with the filter capacitor. This approach, however, cannot be used in because the system efficiency will be sacrificed.

Figure 4(a) shows the load side equivalent circuit when a resistor is connected in parallel with the filter capacitor. Figure 4(b) shows the associated block diagram. As it is shown in this figure, the resistor reduces the current that is flowing into the capacitor by a value that is proportional to the capacitor voltage and inversely proportional to the resistance of the resistor. Thus, instead of using a real resistor, the role of resistor can be replaced by a virtual resistor. The virtual resistor is implemented by using a voltage sensor (that is already available) and an amplifier with a gain that is inversely proportional to the resistance. The output of the amplifier is then used to reduce the filter inductor current as shown in Figure 4(c). By using this virtual resistor, the output voltage response can be written as

$$V_o(s)=\frac{sR/L_r}{s^3CR+s^2+sR\left(C\omega_o^2+\frac{1}{L_r}\right)+\omega_o^2}V_o^r(s)-\frac{R\left(s^2+\omega_o^2\right)}{s^3CR+s^2+sR\left(C\omega_o^2+\frac{1}{L_r}\right)+\omega_o^2}I_o(s) \tag{8}$$

As it is shown by Eq. (8), the output voltage at the desired frequency ω_o is still equal to the desired output voltage but the virtual resistance damps the oscillation.

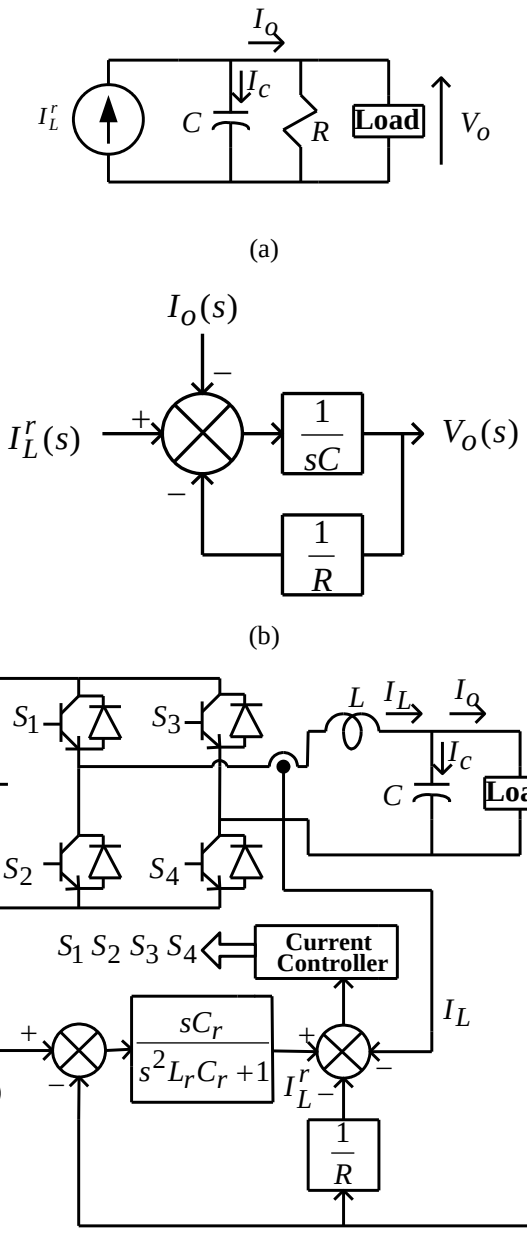


Figure 4 Development of virtual resistance to damp the oscillations.

In Figure 4(c), the virtual resistance responds to the total output voltage. Thus, the virtual resistance responds to both the desired and undesired components of the output voltage. We can design a virtual resistance that responds only to the undesired (error) component of the output voltage. Such virtual resistance is implemented as shown in Figure 5. By using this virtual resistance, the output voltage response can be obtained as

$$V_o(s) = \frac{s^2R + sC\omega_o^2 + R\omega_o^2}{s^3C + s^2R + s\omega_o^2(C_r + C) + R\omega_o^2} V_o^r(s) - \frac{s^2 + \omega_o^2}{s^3C + s^2R + s\omega_o^2(C_r + C) + R\omega_o^2} I_o(s) \tag{9}$$

The control scheme as shown in Figure 5 is the one that will be implemented in the experimental system. Both virtual LC resonant circuit and virtual resistor can be implemented either using analog or digital circuits.

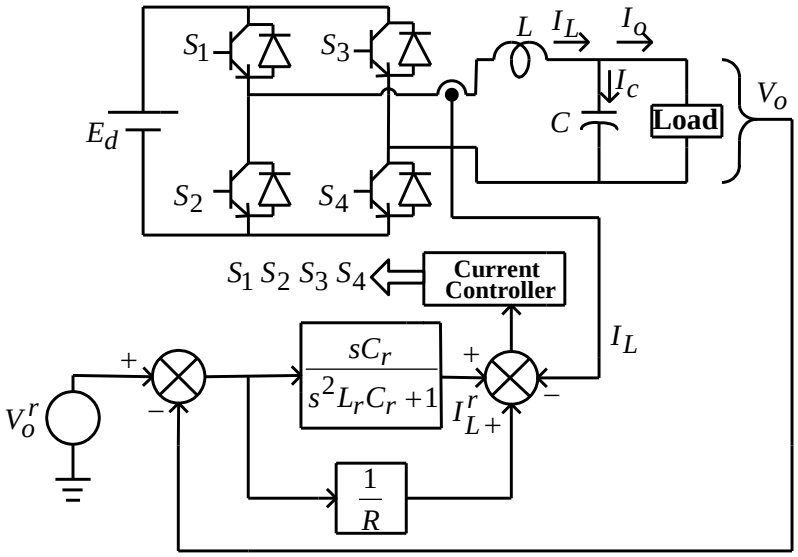


Figure 5 Scheme of the implemented system.

4 Experimental Results

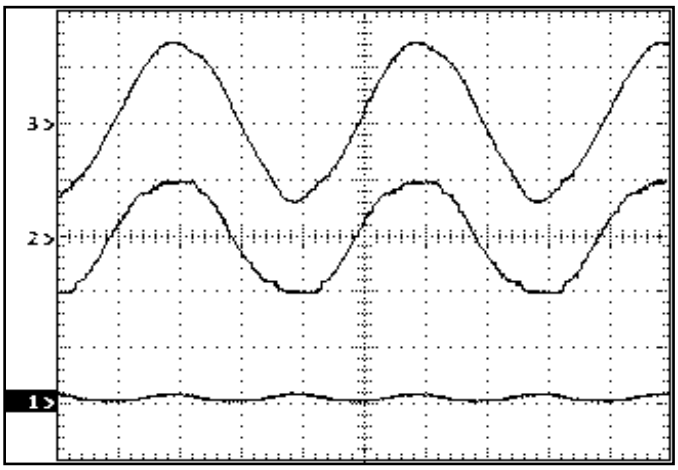
In order to verify the proposed method, a single-phase PWM inverter with the scheme as shown in Figure 5 was constructed. Bipolar junction transistor modules were used as the inverter switching devices. The dc voltage source is obtained from a single-phase ac voltage source by using a single-phase diode bridge rectifier. The dc voltage source is maintained constant at 120 Vdc. The output voltage of the rectifier is smoothed by using a dc filter capacitor of 2200 μF. The output filter inductance is 5 mH and filter capacitance is 200 μF. The width of the smaller hysteresis band is 0.8 A and the larger hysteresis band is 1.2 A.

Though the virtual LC circuit can be implemented by using analog components, a digital implementation is chosen in this experimental system. The virtual LC is implemented by using a DSP of TMS320C542. The virtual LC resonant circuit is tuned at 50 Hz. The inductance and capacitance of the LC resonant circuit are 1 mH and 32 μF, respectively. No attempt has been made to optimize the parameters. The virtual resistor is implemented by using analog electronic components. A virtual resistance of 1 ohm was used in this experiment. A virtual resistance that responds only to the output voltage error signal was used in this experiment.

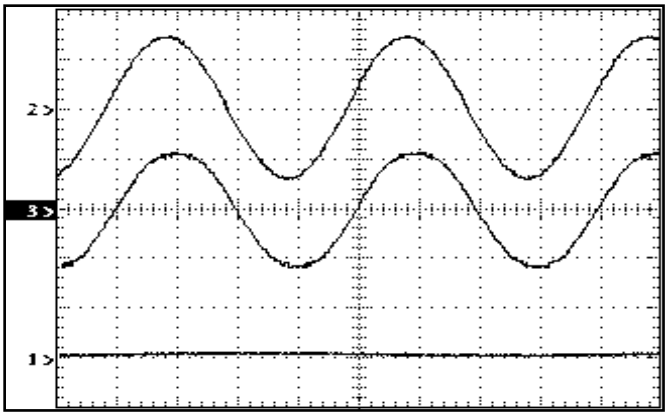
Figure 6(a) shows the experimental result under resistive load when the virtual resistance is not used. The load resistance was 10 ohm. The result shows that a zero steady-state output voltage error can be obtained by the proposed virtual LC resonant circuit. As the damping factor is small, oscillations on the output voltage and current and also on the voltage error signal can be clearly observed. The THD (total harmonic distortion) of the output voltage is 5.3%.

Figure 6(b) shows the result when the virtual resistance is connected. The oscillations on the output voltage and voltage error signal are suppressed. The THD of the output voltage is significantly reduced to 1.1%.

Figure 7 shows the experimental results when the reference voltage is suddenly changed. Without using the virtual resistance, the actual output voltage takes more than one cycle to follow the reference one. When the virtual resistance is used, the output voltage is able to follow quickly the reference voltage. The output voltage transient is damped significantly by using the proposed virtual resistance.



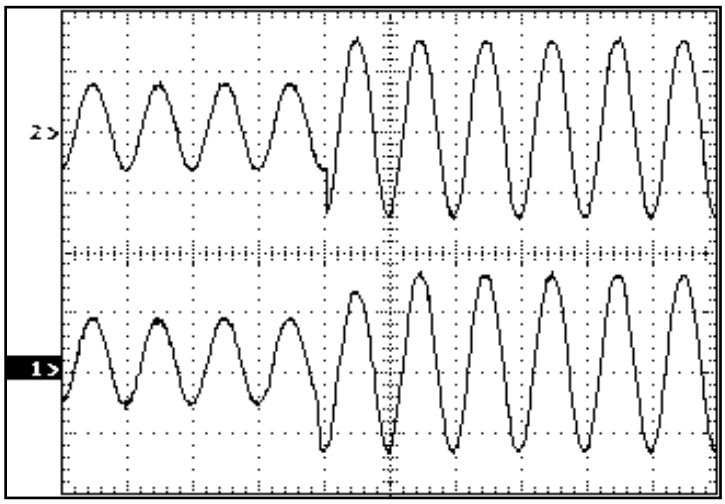
(a)



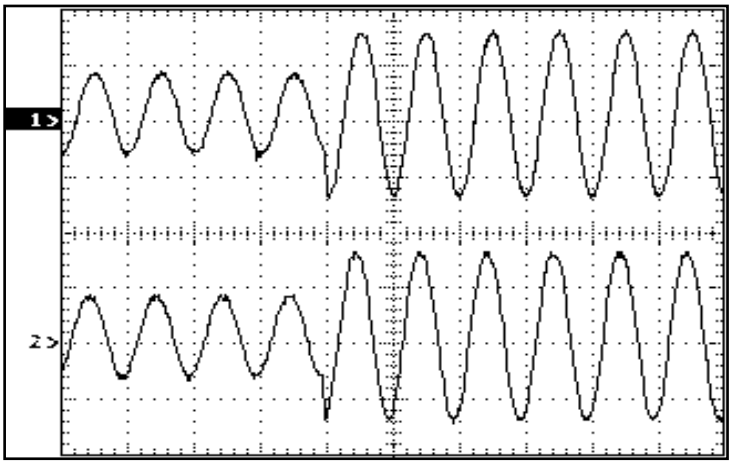
(b)

Upper: Output voltage (50 V/div: 5 ms/div)
Middle: Output current (7 A/div: 5 ms/div)
Lower: Error signal (50 mV/div: 5 ms/div)

Figure 6 Experimental results under resistive load (a) without and (b) with virtual resistance.



(a)

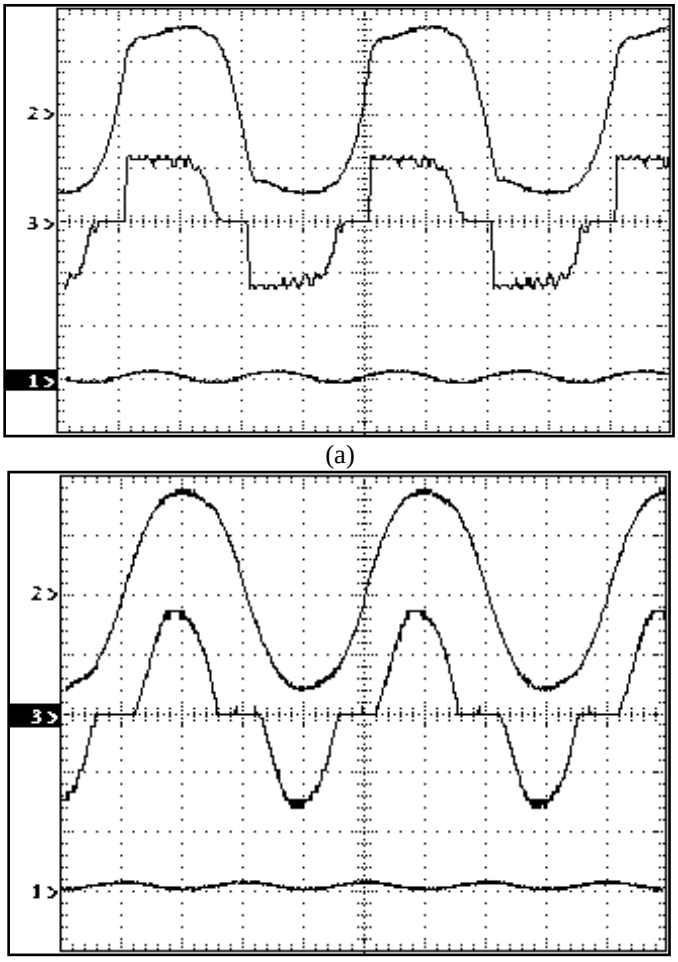


(b)

Upper : Reference voltage (50 V/div : 20 ms/div)
Lower : Actual voltage (50 V/div : 20 ms/div)

Figure 7 Experimental results when the reference voltage is suddenly changed (a) without and (b) with virtual resistance.

Figure 8 shows the experimental results under nonlinear load. A capacitive diode bridge rectifier was used as the load. With this nonlinear load, the load periodically generates transient condition. Without using the virtual resistance, the output voltage is badly distorted because a continuous oscillation is generated. The measured output voltage THD was 19.4%. When the virtual resistance is used, the oscillation is effectively suppressed. The THD on the output voltage is significantly reduced into 4.2%.



Upper : Output voltage (50 V/div : 5 ms/div)
Middle : Output current (7 A/div : 5 ms/div)
Lower : Error signal (50 mV/div : 5 ms/div)

Figure 8 Experimental results under nonlinear load (a) without and (b) with virtual resistance.

5 Conclusions

A new voltage control method for single-phase PWM inverter has been proposed in this paper. The proposed output voltage controller is derived based on virtual LC resonant circuit and virtual resistor. Virtual LC resonant circuit is used to achieve a zero steady-state error and virtual resistor is used to damp the oscillation. Experimental results have shown the validity of the proposed method. Extensions of the proposed controller to other applications are under investigation.

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